IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A method of transferring a data unit from a computer system memory and to an external system through an I/O device using a memory access controller, said memory access controller including a register for storing information which the memory access controller uses to control its own operation, said method comprising the steps of:

a first step, executed by said memory access controller, of retrieving said data unit from said computer system memory and transmitting said data unit to said I/O device;

a second step, executed by said I/O device, of transmitting said data unit retrieved and transmitted in said first step to said external system;

a third step, executed by said I/O device, of sending a data status signal to said memory access controller when said second step is complete; and

a fourth step, executed by said memory access controller, of storing an indication of said data status signal sent in said third step in said register.

2. (Original) A method as in claim 1 wherein said data status signal indicates a successful transmission of said data unit to said external system by said I/O device, wherein said register is a channel status register, and wherein a bit of said channel status register assumes a value indicative of receipt of said data status signal.

3. (Original) A method as claimed in claim 2 wherein said memory access controller waits until said bit reflects a value of said data status signal indicating successful transmission of a data unit to the external system before sending another data unit.

4. (Original) A method as claimed in claim 1 wherein said external system is a network, said I/O device is an Ethernet controller, and said data unit is a packet.

5. (Original) A method as claimed in claim 1 wherein said data status signal is an interrupt signal.

6. (Original) A method as claimed in claim 1 wherein said memory access controller is a DMA channel controller.

7. (Original) A method as claimed in claim 1 wherein there are two DMA channels, a receive channel and a transmit channel, and wherein an interrupt from a said receive channel is masked.

8. (Original) A computer system comprising:

a computer system memory;

an I/O device connected to an external system to transfer data units between said computer system memory and an external system, said I/O device including a data status signal generator which generates a data status signal upon completion of transfer of a data unit;

a memory access controller connected to said computer system memory and said I/O device; said memory access controller including a register for storing status information which the memory access controller uses to control its own operation, wherein said memory access controller receives said data status signal and stores an indication of a value of said data status signal in said register, wherein during a data transmit operation the memory access controller retrieves said data unit from said computer system memory and transfers said data unit to said I/O device and said I/O device transmits said data unit to said external system and wherein the said data transfer status signal is sent from the I/O device to the memory access controller after the transfer of said data unit to said I/O device.

9. (Original) A computer system as claimed in claim 8 wherein said data status signal indicates a successful transmission of a data unit to said external system by said I/O device, wherein said register is a channel status register, and wherein a bit of the channel status register is arranged to reflect a value of said data status signal.

10. (Original) A computer system as claimed in claim 9 wherein said memory access controller waits until said bit reflects a value of said data status signal indicating successful transmission of a data unit to the external system before sending another data unit.

11. (New) The method of claim 1 wherein the data status signal indicates the end of the data unit.

12. (New) The method of claim 1 wherein the data status signal is used to control the operation of the memory access controller.

13. (New) The method of claim 1 wherein the memory access controller executes an instruction in response to the data status signal.

14. (New) The method of claim 1 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

15. (New) The method of claim 1 wherein the data status signal is used to keep a channel process active.

16. (New) The system of claim 8 wherein the data status signal indicates the end of the data unit.

17. (New) The system of claim 8 wherein the data status signal is used to control the operation of the memory access controller.

18. (New) The system of claim 8 wherein the memory access controller executes an instruction in response to receipt of the data status signal.

19. (New) The system of claim 8 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

20. (New) The system of claim 8 wherein the data status signal is used to keep a channel process active.

21. (New) A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer; and

circuitry coupled to the register that receives the data status signal and for controlling subsequent operation of the memory access controller based on the data status signal.

22. (New) The controller of claim 21 wherein the data status signal indicates an end of the data unit.

23. (New) The controller of claim 21 wherein the memory access controller executes an instruction in response to the data status signal.

24. (New) The controller of claim 21 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

25. (New) The controller of claim 21 wherein the data status signal is used to keep a channel process active.

26. (New) A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system; and

means for controlling subsequent operation of the memory access controller using the data status signal.

27. (New) The memory access controller of claim 26, wherein the data status signal indicates an end of the data unit.

28. (New) The memory access controller of claim 26, wherein the memory access controller further comprises:

means for executing an instruction in response to the data status signal.

29. (New) The memory access controller of claim 26, wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

30. (New) A memory access controller adapted to be coupled to a memory of a computer system, comprising:

a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system; and

a circuit capable of using the status data.

31. (New) The memory access controller of claim 30, where the I/O device generates the status data after a data unit transfer from the computer system memory to the system external to the computer system.

32. (New) The memory access controller of claim 30, wherein the circuit is capable of using the status data to control any subsequent data unit transfers between the computer system memory and the system external to the computer system.

33. (New) The memory access controller of claim 30, wherein the memory is configured to store status data is a register and the computer system is a computer.

34. (New) A data transmission method, comprising:

transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device;

generating status data using the I/O device, the status data indicating completion of the data unit transfer;

storing the status data in the memory; and

using the status data to control subsequent operation of the memory access controller.

35. (New) The data transmission method of claim 34, wherein the status data indicate completion of a data unit transfer from the memory in the computer system to the system external to the computer system.

36. (New) The data transmission method of claim 34, further comprising:

determining whether the status data in the memory indicate completion of the data unit transfer; and

transferring another data unit between the memory in the computer system and the system external to the computer system after determining that the data in the memory indicate completion of the data transfer.